Panel Sessions

1. **Topic**: Chiplet Integration – Chiplet Integration combines small, modular chips to form a larger, more complex system-on-a-chip (SoC). It is a promising method to extend Moore's Law and continue the trend of improving performance while reducing or maintaining costs in the semiconductor industry. Compared to the traditional monolithic integration, chiplet integration can offer multiple advantages such as design flexibility, better performance and lower cost. However, this technology is not yet widely adopted by the industry. To improve its maturity, there are still many challenges such as packaging issues, new materials, interconnect technologies, as well as testing coverage. This panel session brings together the experts from the industry and academia to discuss those challenges and opportunities.

   Moderator: Dr. Jiantao Zheng, HiSilicon

   Dr. Jiantao Zheng is the Chief Engineer in the Packaging Design Department at HiSilicon. He has been working in the Microelectronics Packaging areas for over 20 years. He supervised the Packaging Core Competency teams including 2.5D/3D integration, thermal mechanical design, chip-packaging interaction, materials applications, substrate technologies, and characterization laboratories, etc. He had over 20+ technical publications and over 50+ patents, he has a PhD degree from Georgia Tech.

   Panellists:

Dr. Ravi Mahajan is an Intel Fellow responsible for Assembly and Packaging Technology Pathfinding for future silicon nodes. Ravi also represents Intel in academia through research advisory boards, conference leadership and participation in various student initiatives. He has led Pathfinding efforts to define Package Architectures, Technologies and Assembly Processes for multiple Intel silicon nodes including 90nm, 65nm, 45nm, 32nm, 22nm and 7nm silicon. Ravi joined Intel in 1992 after earning his Ph.D. in Mechanical Engineering from Lehigh University. He holds the original patents for silicon bridges that became the foundation for Intel's EMIB technology. His early insights have led to high-performance, cost-effective cooling solutions for high-end microprocessors and the proliferation of photo-mechanics techniques for thermo-mechanical stress model validation. His contributions during his Intel career have earned him numerous industry honors, including the SRC's 2015 Mahboob Khan Outstanding Industry Liaison Award, the 2016 THERMI Award from SEMITHERM, the 2016 Allan Kraus Thermal Management Medal & the 2018 InterPACK Achievement award from ASME, the 2019 "Outstanding Service and Leadership to the IEEE" Awards from IEEE Phoenix Section & Region 6 and most recently the 2020 Richard Chu ITherm Award and the 2020 ASME EPPD Excellence in Mechanics Award. He is one of the founding editors for the Intel Assembly and Test Technology Journal (IATTJ) and currently VP of Publications & Managing Editor-in-Chief of the IEEE Transactions of the CPMT. He has long been associated with ASME's InterPACK conference and was Conference Co-Chair of the 2017 Conference. Ravi is a Fellow of two leading societies, ASME and IEEE. He was elected to the National Academy of Engineering in 2022

for contributions to advanced microelectronics packaging architectures and their thermal management

Dr. Surya Bhattacharya (Senior Member IEEE) is Director and Head of System-in-Package at A*STAR Institute of Microelectronics (IME), Singapore. At the Institute of Microelectronics, Singapore, Dr. Bhattacharya leads the advanced packaging team to initiate and execute consortia projects to address industry challenges in advanced heterogeneous integration for system scaling. Prior to joining IME, he served as Director of Foundry Engineering at Qualcomm, where he executed technology and manufacturing ramps across multiple foundries around the world. Surya has a PhD in Electrical Engineering from the University of Texas at Austin, and B.Tech in Electrical Engineering from the Indian Institute of Technology, Madras.

Dr. Arvind Sundarrajan is the Managing Director/Head of Applied Packaging Development Center (APDC) - the Center of Excellence for Advanced Packaging for Applied Materials in Singapore. He was appointed as company director of Applied Materials Singapore Technology Pte Ltd since 2015.

He brings extensive experience and expertise to his role, where he manages all product development for Applied Materials' Advanced Packaging Development Center, a $450M joint lab with A*STAR's Institute of Microelectronics. He is responsible for R&D, concept & feasibility, prototype design and testing, product releases as well as customer management. He is also leading the development of partnerships with research institutes across Asia to develop new concepts and drive disruptive innovation at Applied Materials.

Dr. Sundarrajan has had notable successes in his R&D career. He has successfully released several products in the areas of physical vapour deposition, chemical vapour deposition, atomic layer deposition and contact-clean technologies. He has numerous patents to his credit and has published several papers.

Dr. Sundarrajan currently serves on the Industry Advisory Board (IAB) of the Department of Materials Science, National University of Singapore (NUS) and on the Industrial Advisory Committee (IAC) at the School of Materials Science and Engineering at Nanyang Technological University (NTU). He has served as a member of Governing Board of the Singapore Synchrotron Light Source (SSLS) and NUS Nanoscience and Nanotechnology Initiative (NUSNNI). He was also a member of the Technical Review Committee for Advanced Packaging (SEMI SEA).

Dr. Sundarrajan joined Applied Materials in 1996 and has held several management roles in the last 27 years. He has a Ph.D. in Materials Science and Engineering from the Massachusetts Institute of Technology (MIT), Cambridge, USA.

Dr. Chih Pin Hung currently holds the position of Vice President, Corporate R&D, at ASE Group. Based in Taiwan, he leads teams responsible for next-generation product development featuring integrated technologies, as well as a broad range of advanced chip, package, and system integration solutions. During his tenure, Dr. Hung has performed a variety of management roles at ASE, including VP of Corporate Design, VP of Central Engineering & Business Development and VP of Logistic Services Integration. He holds 180 patents encompassing IC packaging structure, process, substrate, and characterization technology. He has also published over 105 conference and journal papers. Dr. Hung has been the SEMICON Taiwan PKG & TEST Committee Chair since 2013, and currently Co-Chair since 2021. He is also a member of the IEEE EPS Board of Governor since 2019.

2. **Topic**: Artificial Intelligence for Package Design and Manufacturing - Artificial Intelligence has the potential to transform industries, improve quality of life, and address global challenges by leveraging data-driven insights, automation, and intelligent decision making. This panel discussion will focus on how the power of AI can be harnessed to benefit the IC Packaging industry. Industry experts from the fields of Package Design, Equipments, Substrate Manufacturing and Factory Automation will discuss the opportunities, benefits and challenges in using AI for IC Package Design & Manufacturing.

   Moderator: Dr. Sam Karikalan, Broadcom Inc., Vice President of Conferences - IEEE EPS

   Dr. Sam Karikalan is the Vice President of Conferences at the IEEE Electronics Packaging Society. He has been with Broadcom for the 18+ years, currently as Sr R&D Manager responsible for Package Technology Pathfinding and Design Optimization. His areas of interests are Heterogeneous Integration, Advanced Substrate Technologies, Package Design for Performance Scaling, Supply Chain Development and use of AI for Package Design & Manufacturing.

   Sam worked for STATS ChipPAC, Primarion, AMD and SAMEER-Centre for Electromagnetics for 17 years before joining Broadcom. He has 23 issued and 15 pending US patents to his credit, besides several publications in international journals and conferences. Sam has a Bachelor of Engineering degree from Coimbatore Institute of Technology and received UNIDO Fellowship training in EMI/EMC from Interference Control Technologies, Gainesville, VA.

   Panellists:

Mr. Vincent has over 33 years' experience in Technology Development, Operations, Business, Sales and Marketing, having demonstrated success at companies like IBM, Amkor, ASE, TSMC, and GLOBALFOUNDRIES. Vincent joined Applied Materials in 2016.

Currently leading Corporate and Business Development for the Advanced Packaging and ICAPS division at Applied Materials, he is responsible for forging new strategic alliances and partnerships key to technology advancement for future product solutions. Vincent leads all aspects of critical technology inflections related to Heterogenous Integrated, next generation integration of Silicon, volumetric scaling for all key aspects of the technology stack related advanced packaging; 3DIC Heterogenous Integration.

With a degree in Pure and Applied sciences at Champlain Regional College, and a Bachelor of Engineering degree from Concordia University, Vincent is both the author and co-author of 40+ Patents in the field of advanced semiconductor packaging and heterogenous integration.

Ms. Grace has been with iNEMI in Europe since 2007. Prior to becoming Vice President, Grace was iNEMI's Manager of European Operations and then Managing Director-EMEA. In these roles, she was responsible for interactions with iNEMI members in the region, as well as interfacing with the larger technical community in Europe. She managed all European activities for the consortium, including organizing workshops and forums, engaging participation in and promoting the iNEMI roadmap and collaborative projects.

Her background is in materials and manufacturing research. Prior to joining iNEMI, the majority of her career was spent at Motorola. While there, she worked initially on the development of direct chip attach (DCA)/flip chip capabilities and low-cost assembly processes. In later years she worked as a program manager, interfacing with various business units to help develop and qualify suppliers and to transfer low-cost assembly processes into volume production. She also spent two years establishing and leading a multidisciplinary research team at Motorola's site in Jaguariuna, Brazil, supporting the volume manufacturing of cell phones, radios and cellular infrastructure for the Latin America markets.

Prior to Motorola, Grace was a research engineer for the National Microelectronics Research Center (now the Tyndall National Institute) in Cork, Ireland. She worked on projects for the European Space Agency, focusing on the assembly of high-reliability packaging for aerospace applications. Grace has an honors bachelor's degree in electrical engineering from University College Cork (Ireland), and a master of science in materials and

manufacturing engineering from the Illinois Institute of Technology (Chicago, U.S.A.). She has authored presentations for many conferences including IEEE-CPMT, ITAP and ECTC. She holds eight U.S. patents, and is a member of IEEE.

Mr. Samuel joined Kulicke & Soffa in the year 2014 as a Senior Director of the Advanced Packaging business unit. In his role, he is responsible for the business development of the Advanced Packaging product portfolio and has successfully led the business unit to penetrate the mobile chipset manufacturing high bandwidth Package on Package (HBPoP) for key customers in Asia. As an industry veteran, Samuel has more than 20 years of project and product management experience in the mid to large-scale capital equipment industry. Before joining K&S, he held positions in various companies such as KLA-Tencor and Flextronics.

Most recently, he was appointed as the Vice Chairman of the Advanced Packaging Forum for SEMICON SEA 2023.

Samuel holds an Honors Bachelor's degree in Mechanical Engineering from the University of Sheffield.

Mr. Gopal Garg is EVP (Marketing and Application Engineering) at SEMCO San Jose USA. Since 2015 at SEMCO, he is responsible to work with key customers (Semiconductors, Clients / HPC Computation, Mobile platforms and Automotive) to grow of SEMCO across all product lines (Substrates, Camera Modules and Passive Components). During his career he has worked in leadership positions as SVP/GM in public companies like Cypress Semiconductor, Synaptics, Sun Power Corporation and start-up companies like Arcus Technology and SCL. In addition, he has served on the advisory board of Public and Private Companies. In his various roles as GM, he has organically grown and managed yearly revenue from scratch to $2B and acquired / invested / integrated in over 20 companies. Gopal Garg is a graduate in Electrical engineering from BITS Pilani India and MBA from Chandigarh India.

Professor Kuo Ning Chiang received his PhD from the Georgia Institute of Technology, USA. He is the Chair Professor at the National Tsing Hua University in Hsinchu, Taiwan. After graduating from Georgia Tech, he worked four years as a senior researcher at MSC/NASTRAN, a world-famous finite element system. From 2010 to 2013, he served as General Director of the National High-Performance Computing Center, which is the National Strategic Research Center of Taiwan. He has received outstanding research awards from the Ministry of Science and Technology of Taiwan three times and has published more than 450 technical papers in international journals and conference proceedings. He has been granted more

than 50 invention patents. Among the major awards Professor Chiang received are the Excellence in Mechanics Award from ASME (2022) and the Outstanding Sustained Technical Contribution Award (2020) from IEEE-EPS. Currently, he is Editor-in-Chief of the Journal of Mechanics (SCI), Academic Editor of Materials (SCI), and Associate Editor of the Journal of Electronic Packaging (SCI). He is an IEEE, ASME, STAM, and IMAPS Fellow. And an academician of the International Academy of Engineering (IAE).

He has made significant achievements in simulation-based science and technology. He successfully combined simulation design with artificial intelligence technology and applied it effectively to semiconductor-related designs. His technology has greatly reduced product development time and development costs. He has worked with many major electronic packaging, semiconductor and LED companies such as ACET, TSMC, MediaTek, UMC, EPISTAR, VIA, Powertech Technology, etc.